



Tanta University



Faculty of Engineering

**Electrical Power and Machines
Engineering Department**

Electric Circuit (1) Lab Experiments

**1st Year of Electrical Engineering
1st Term**

The slide features decorative wavy lines in yellow and brown. A thick yellow line curves across the top and bottom of the text area. A thinner, lighter yellow line follows a similar path just below the first one. At the very bottom, there is a solid dark brown wavy shape.

Experiment (2)

Kirchhoff's Voltage Law

Kirchhoff's Voltage Law

- K.V.L. states that the summation of **voltage rises** is equal to the **voltage drops** in a closed loop in any electrical circuit.

$$\sum V_{\text{rises}} = \sum V_{\text{drops}}$$

OR:

- The summation of all voltages in any closed loop is equal to zero.

$$\sum V = 0$$

Objective of experiment

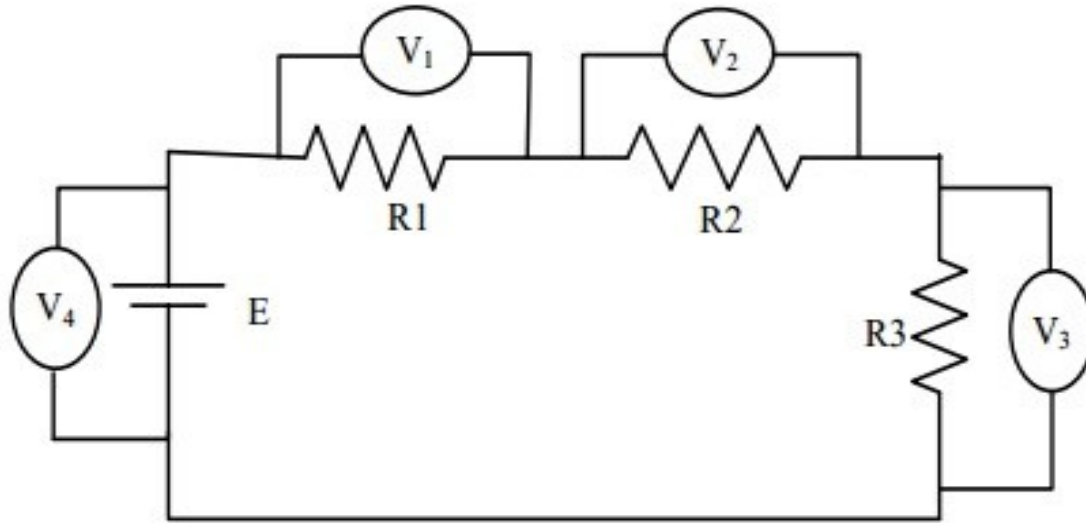
- To verify experimentally K.V.L. for a simplified electrical circuit.

Experiment Requirements

- 3 Resistors.
- D.C. Supply.
- 4 D.C. Voltmeters.



Experiment connection



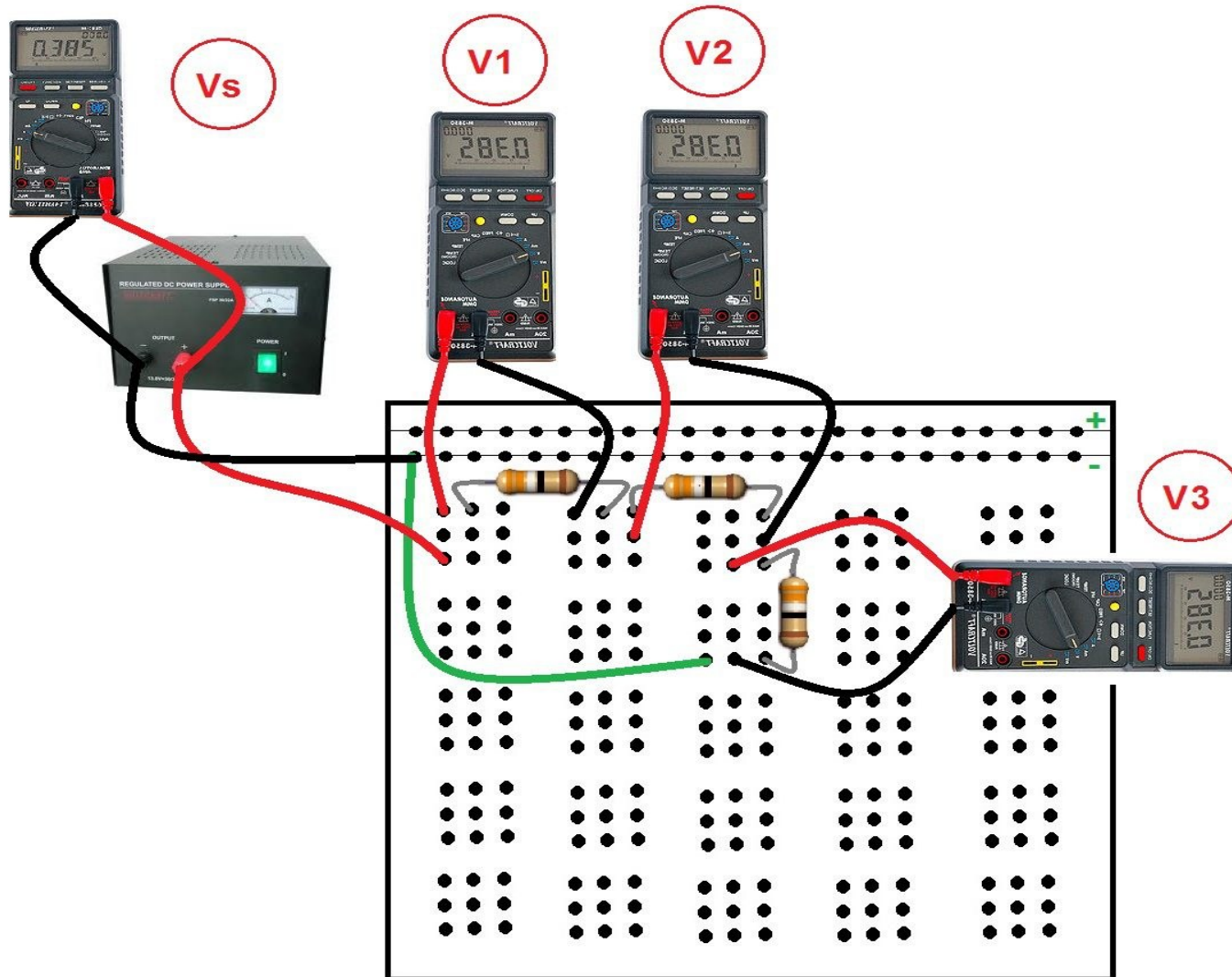
It is supposed to note that:

$$\mathbf{E=V1+V2+V3}$$

OR

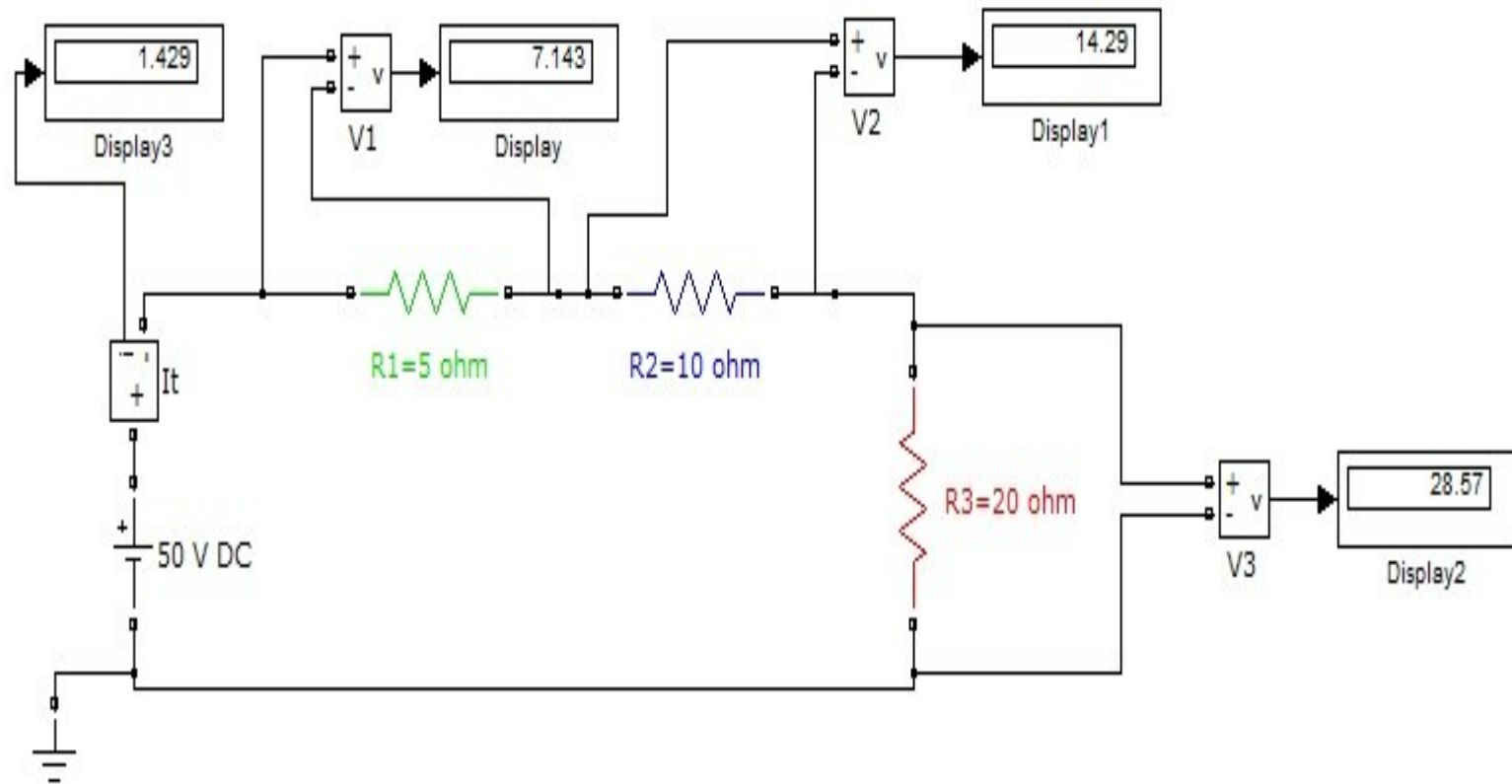
$$\mathbf{E-V1-V2-V3=0}$$

Experiment connection



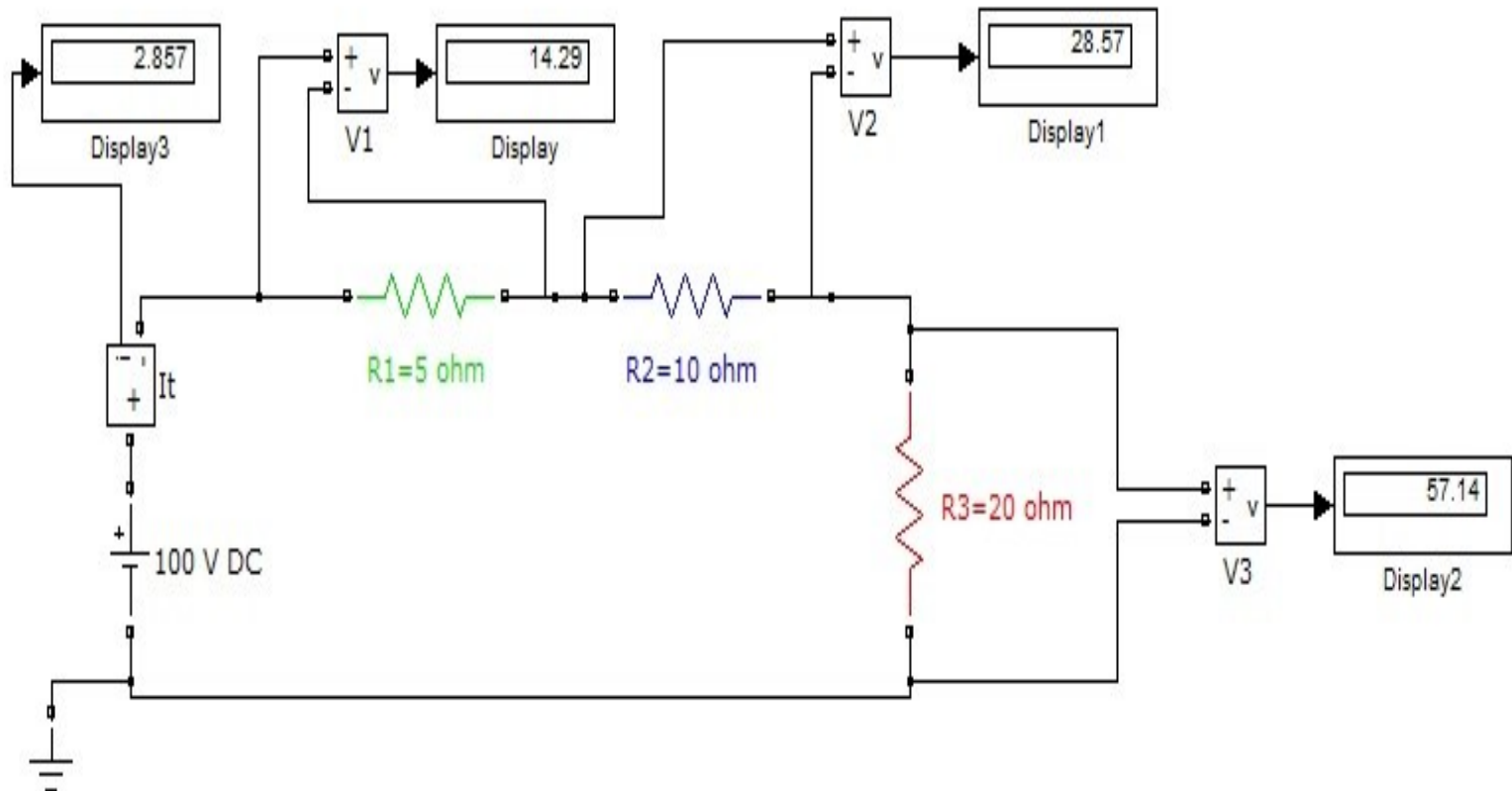
Simulation results

At Supply voltage = 50 V



Simulation results

At Supply voltage = 100 V



Experiment results

By changing the D.C. Source value, then read the rest of voltages and record it.

VS	V1	V2	V3